

## CLAIMS

What is claimed is:

- 1 1. A computer system, comprising:
- 2 a processor comprising a cache, a first bus interface and a second bus
- 3 interface; and
- 4 a controller to snoop the cache via the first bus interface during a first
- 5 mode of operation and to snoop the cache via the second bus
- 6 interface during a second mode of operation.
- 1 2. The computer system of claim 1, further comprising a first bus to couple the
- 2 first bus interface to the controller, and a second bus to couple the second
- 3 bus interface to the controller, the first bus being wider than the second bus.
- 1 3. The computer system of claim 2, further comprising a main memory and a
- 2 peripheral device, the peripheral device to request an access of the main
- 3 memory via the controller.
- 1 4. The computer system of claim 1, further comprising a main memory and a
- 2 peripheral device, the peripheral device to request an access of the main
- 3 memory via the controller.
- 1 5. The computer system of claim 1, wherein the first mode of operation is a high
- 2 power mode and the second mode of operation is a low power mode.



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3 controller via a second bus, and the first bus consumes more power during  
4 the first mode of operation than the second bus consumes during the second  
5 mode of operation.

1 11. The computer system of claim 1, wherein the second bus interface is coupled  
2 to the controller via a second bus, and the second bus includes a clock signal  
3 line for source-synchronous operation, a control line, and a data line.

1 12. The computer system of claim 11, wherein the first bus interface is coupled to  
2 the controller via a first bus, the first bus is a parallel bus, and the second bus  
3 is a serial bus having a single data line.

1 13. A computer system, comprising:  
2 a high power bus;  
3 a low power bus that is narrower than the high power bus and includes a  
4 clock signal line for source-synchronous operation;  
5 a processor comprising a cache, a high power bus interface coupled to  
6 the high power bus and a low power bus interface coupled to the low  
7 power bus; and  
8 a controller to communicate with the processor via the high power bus  
9 during a high power mode of operation and to communicate with the  
10 processor via the low power bus during a low power mode of  
11 operation.

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- 1 14. The computer system of claim 13, further comprising a main memory and a  
2 peripheral device, the peripheral device to request an access of the main  
3 memory via the controller.
- 1 15. The computer system of claim 13, wherein the high power bus is to be  
2 powered down during the low power mode of operation.
- 1 16. The computer system of claim 13, wherein the controller is to snoop a  
2 memory region of the processor via the high power bus during the high power  
3 mode of operation, and the controller is to snoop the memory region via the  
4 low power bus during the low power mode of operation.
- 1 17. The computer system of claim 16, further comprising a clock generator, the  
2 clock generator to provide a clock signal to the memory region via a first clock  
3 signal line coupled between the clock generator and the processor during the  
4 high power mode of operation, the clock generator to further provide a clock  
5 signal to the memory region via the clock signal line of the low power bus  
6 during the low power mode of operation.
- 1 18. The computer system of claim 13, wherein a clock signal is to be provided via  
2 the clock signal line by the controller.



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1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100

1 24. The integrated circuit of claim 21, wherein the low power bus interface  
2 provides for source-synchronous operation and the high power bus interface  
3 lacks support for source-synchronous operation.

1 25. The integrated circuit of claim 21, further comprising a first phase-locked loop  
2 (PLL) to provide a clock signal to the memory region during the high power  
3 mode of operation, and a second PLL to provide a clock signal to the memory  
4 region during the low power mode of operation, the second PLL to receive a  
5 clock signal via the low power bus interface.

1 26. The integrated circuit of claim 21, further comprising a memory bus interface.

1 27. A method of accessing a cache comprising:  
2 snooping a cache via a high power bus during a high power mode of  
3 operation;  
4 transitioning to a low power mode of operation; and  
5 snooping the cache via a low power bus during a low power mode of  
6 operation.

1 28. The method of claim 27, wherein transitioning to a low power mode of  
2 operation includes powering down the high power bus.

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1 29. The method of claim 27, wherein snooping the cache via the low power bus  
2 includes providing a clock signal to the cache via the low power bus.

1 30. The method of claim 27, wherein transitioning to the low power mode of  
2 operation includes flushing a cache.

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